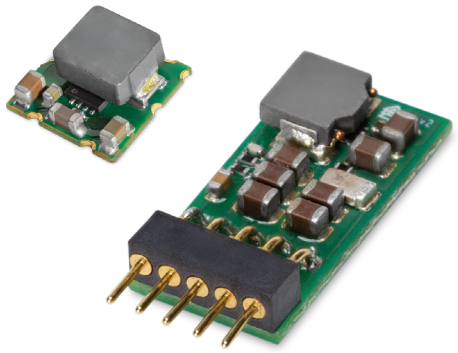
voltbricks

DATASHEET

# VNA3 «EULER» Series

Non-isolated switching voltage regulator with integrated inductor

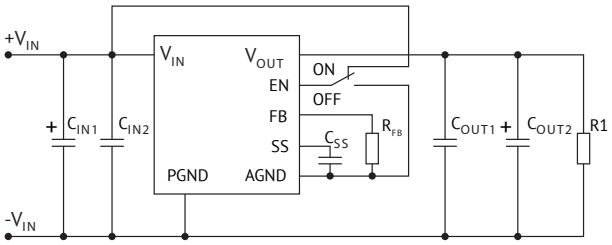


## 1. Features

- Input voltage range 4,5 to 18 VDC
- Adjustable output voltage from 0,765 to 7 V
- Output current up to 3 A
- Low profile design - height 3,3 mm max
- Switching frequency 700 kHz
- Weight 0,4 g max

## 2. Advantages

- Compact size
- Integrated inductor
- Minimum external components
- High efficiency
- Ultrafast response to load changes
- Low power consumption at no-load and standby mode
- Remote On/Off and soft start
- SCP and OCP




VNA3 typical circuit.

## 3. Description

**Switching voltage regulator of the VNA3 «EULER» series** - the first of compact solutions for telecommunications and general industrial applications from a leading developer and manufacturer of power supply systems and components - VOLTBRICKS company.

Turnkey solution based on VNA3 «EULER» and its' typical connection components cover not more than 200 $mm^2$ of PCB. It means that EULER is one of the smallest miniature step-down voltage regulator produced at the moment.

VNA3 is based on a high-efficient controller with integrated MOSFET transistors. These components are connected in a synchronous rectification circuit and optimized for light-load operation. This design achieves 93 % peak efficiency at 50 % load, and 90 % efficiency at 10 % load, which is comparable with world equivalents.

The converter is designed according to the application features inside of portable devices - for example, low current consumption in standby mode. Typical current in standby mode is 2 µA (maximum 15 µA).

Low-profile design with a 3,3 mm height allows to mount VNA3 in space between printed circuit boards of electronic equipment. It helps to provide a design flexibility and a high density of electronic components.

Soft start and remote control features enable to design different distributed power architectures, without reference to the input overload capacity restrictions, and, for example, to avoid overload or short circuit protections operation of DC-DC converter, which is powering the group of several VNA.

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# 4. Content



# 5. Part number

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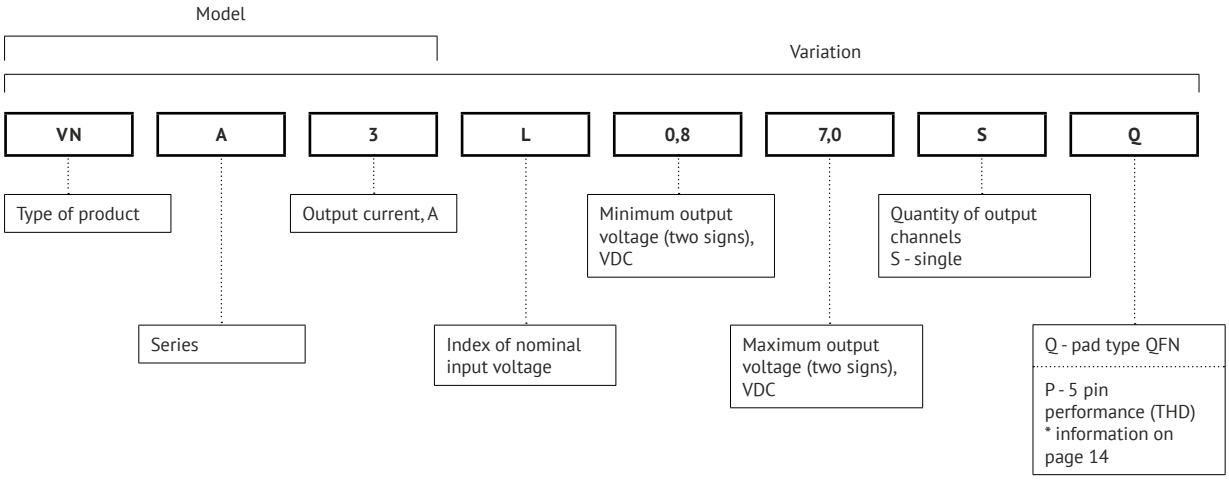
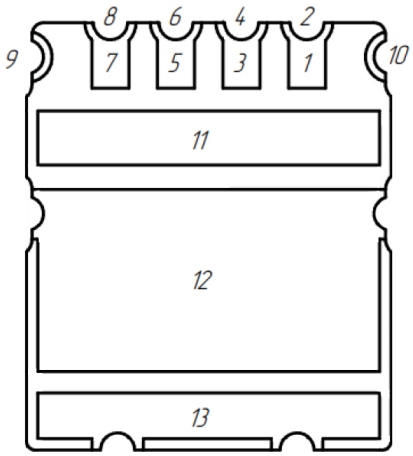


# 6. Pinout

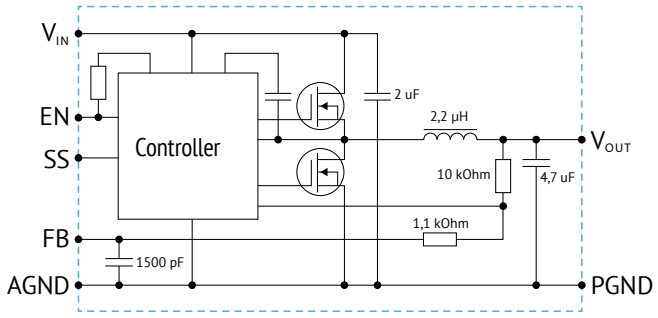



*Pic. 1. EULER pinout (bottom view).*

| Pin name | Pin location | Pin assignment |
|---|---|---|
| AGND | 1, 2 | Analog ground, zero voltage reference for EULER internal circuits and for return of EN (On/Off), SS (Soft start), FB (Feedback input) external circuits. It is not allowed to connect this pin with PGND pins by external circuit, as this connection is made inside of the converter. |
| EN | 3, 4 | Pin On / Off. Low signal on this pin (0,3 V or less), referred to AGND pin turns off the module. A high level signal (2,2 V ... $V_{IN}$), referred to AGND pin, turn it on. |
| FB | 5, 6 | Converter's feedback input. The output voltage depends on the resistance of the resistor connected between this pin and AGND pin. |
| SS | 7, 8 | Pin of the soft start time setting. The output voltage rise time can be set by capacitor connected between this pin and AGND pin. |
| $V_{OUT}$ | 9, 10, 11 | Output voltage. External output capacitors and load are connected between these pins and PGND pin, close to converter. |
| PGND | 12 | Power ground, converter's power stage current return. The negative circuits of input ($C_{IN}$) and output ($C_{OUT}$) capacitors are connected between this group of pins and the groups $V_{IN}$ and $V_{OUT}$, respectively. PGND pin is also used to improve the heat dissipation efficiency of converter. Therefore, it is recommended to make several vias on the PCB of end-device, which will connect PGND circuit on opposite sides of this board, to improve thermal characteristics. |
| $V_{IN}$ | 13 | Input voltage. External input capacitors are connected between these pin and PGND pin, close to converter. |

# 7. Characteristics

## 7.1. Simplified layout




*Pic. 2. Simplified layout.*

## 7.2. Absolute maximum ratings

| Parameter | Designation | Min. | Max. | Unit of measurement |
|---|---|---|---|---|
| Input voltage | $V_{IN}$ | −0,3 | +20 | VDC |
| Voltage at EN pin | $V_{EN}$ | −0,3 | $V_{IN}$ | VDC |
| Voltage at SS pin | $V_{SS}$ | −0,3 | +7 | VDC |
| Voltage at FB pin | $V_{FB}$ | −0,3 | +5,25 | VDC |
| Junction operating temperature[1] | $T_J$ | −40 | +150 | °C |
| Storage temperature | $T_S$ | −60 | +125 | °C |

## 7.3. Recommended operating modes

| Parameter | Designation | Min. | Typical | Max. | Unit of measurement |
|---|---|---|---|---|---|
| Input voltage | $V_{IN}$ | 4,5 | 12 | 18 | VDC |
| Ambient operating temperature | $T_A$ | −40 | – | +85[2] | °C |
| Output current | $I_{OUT}$ | 0 | – | 3 | A |
| Output voltage range | $V_{OUT}$ | 0,765[3] | – | 7[4] | VDC |

## 7.4. Electrical characteristics

Tests passed in a following conditions (unless otherwise indicated):

$T_A$ = 25 °C,
$V_{IN}$ = 12 V,
$V_{EN}$ = 12 V,
$V_{OUT}$ = 5 V,
$I_{OUT}$ = 3 A,
$C_{IN1}$ = 22 uF, 25 V, 1210 ceramic;
$C_{IN2}$ = 270 uF, 35 V, polymer;
$C_{OUT}$ = 2 × 22 uF, 25 V, 1210 ceramic;

| Parameter | Measuring conditions | Min. | Typical | Max. | Unit of measurement |
|---|---|---|---|---|---|
| **Input characteristics** | | | | | |
| Undervoltage protection limit | $V_{IN}$ increases | 3,4 | 3,8 | 4,2 | VDC |
| Undervoltage protection hysteresis | $V_{IN}$ decreases | 200 | 300 | 400 | mV |
| Standby mode current consumption | $V_{EN}$ = AGND | – | 2 | 15 | µA |
| No-load current consumption | $I_{OUT}$ = 0 A | | 1 | | mA |
| **Output characteristics** | | | | | |
| Voltage regulation at Vin gradual change | $V_{IN}$ = 8...18 VDC | | 0,5 | | % |
| Voltage regulation at Iout gradual change *[Pic. 3]* | $I_{OUT}$ = 0...3 A<br>$I_{OUT}$ = 0,8...3 A | | 1,5<br>0,24 | | %<br>% |
| Ripple and noise (p-p) | For a bandwidth of 20 MHz | | 16 | | mV |
| Overcurrent protection limit | | | 5 | | A |
| **Reference voltage source** | | | | | |
| Reference voltage | | 0,753 | 0,765 | 0,777 | VDC |
| **On/off function (EN pin)** | | | | | |
| Guaranteed low level voltage | Referred to AGND pin | 0 | | 0,3 | VDC |

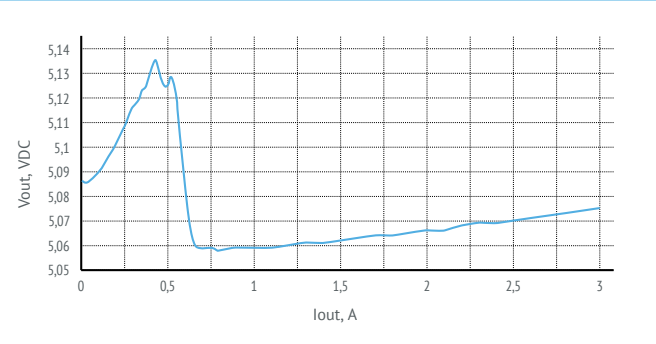
[1] Junction temperature - temperature of converter's IC junction. Ambient temperature - ambient air temperature. The values are given for natural cooling of converter, mounted on a four-layer PCB with dimensions of at least 100×100 mm with a copper thickness of 70 µm.

[2] Subject to the condition $T_J$ <+150 °C.

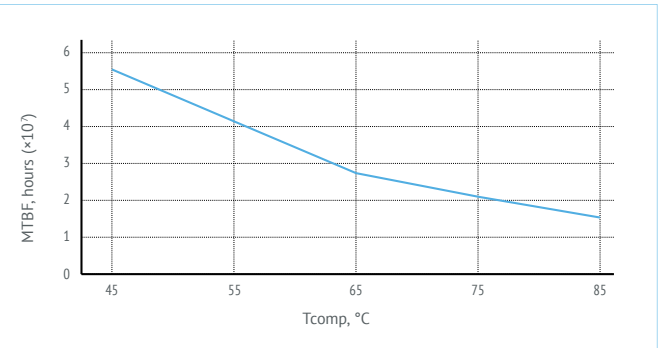
[3] Subject to the condition $V_{OUT} \geq V_{IN} \times 0{,}07$ (V).

[4] Subject to the condition $V_{OUT} \leq V_{IN} \times 0{,}65$ (V).

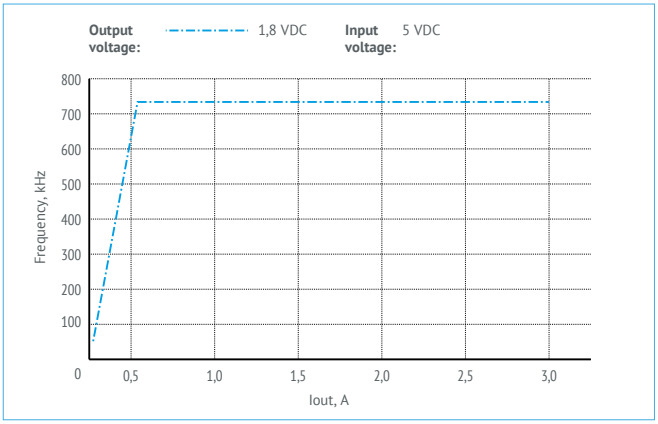
| Parameter | Measuring conditions | Min. | Typical | Max. | Unit of measurement |
|---|---|---|---|---|---|
| Guaranteed high level voltage | Referred to AGND pin | 2,2 | | $V_{IN}$ | VDC |
| Sink current | 5,5 VDC ⩽ $V_{EN}$ ⩽ $V_{IN}$ | | | 300 | uA |
| Source current | 2,2 VDC ⩽ $V_{EN}$ ⩽ 3,0 VDC | | | 70 | uA |
| Sink current | $V_{EN}$ ⩽ 0,3 VDC | | | 7 | uA |
| **Soft start function (SS pin)** | | | | | |
| Charging current | | 1,4 | 2,0 | 2,6 | uA |
| Discharging current | $V_{SS}$ = 0,5 VDC | 0,1 | 0,2 | – | mA |
| **Switching frequency** | | | | | |
| | $I_{OUT}$ = 0...0,6 A | 10 | | 710 | kHz |
| | $I_{OUT}$ = 0,6...3 A | 700 | | 720 | kHz |




*Pic. 3. $V_{OUT}$ vs. $I_{OUT}$ typical curve. $V_{IN}$ = 12 VDC; Vout = 5 VDC.*

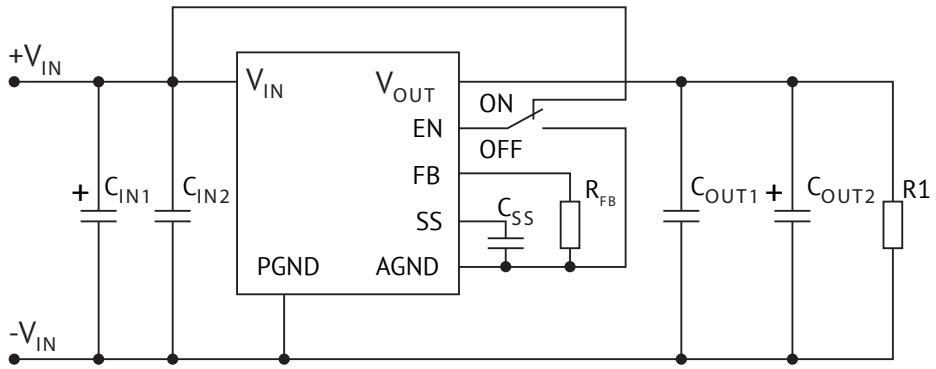



*Pic. 4. MTBF vs. components temperature ($T_{COMP}$) curve. MIL-STD-217F, group Gb.*




*Pic. 5. The dependence of the conversion frequency on the load current.*

# 8. Typical connection diagram




*Pic. 6. Typical connection diagram*

**Table 1.** Description of connection diagram elements.

| | | |
|---|---|---|
| Cin1 | tantalum capasitor | 270 µF |
| Cin2 | ceramic capacitor | 22 µF |
| Cout1 | tantalum capasitor | 47 µF |
| Cout2 | ceramic capacitor | 44 µF |

$C_{SS}$ value is specified in *[10.3]*

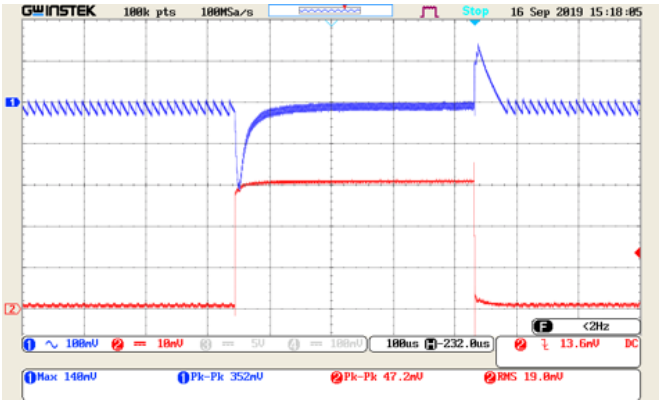
$R_{FB}$ value is specified in *[10.1]*

# 9. Test results

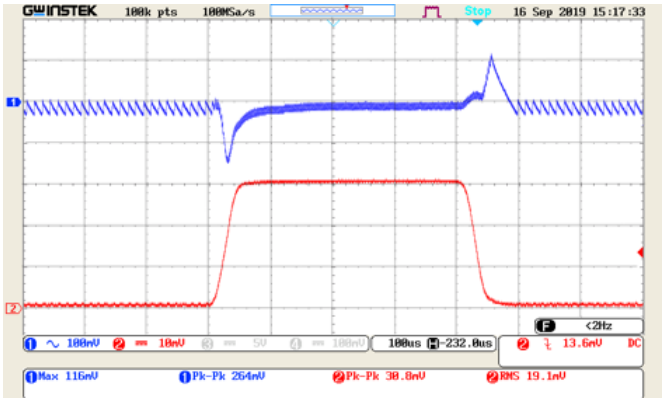
Tests of attached results in paragraphs *[9.1]* and *[9.2]* were carried out according to connecting diagram of VNA3L0,87,0SQ, which is shown in *[Pic. 6]*.

## 9.1. Oscillograms

### 9.1.1. Load transient




*Pic. 7. $I_{OUT}$ = 0,1-3 A; 6,5 A/µs.*

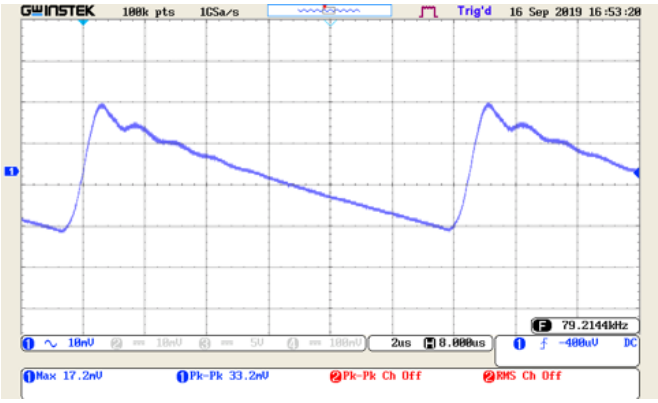



*Pic. 8. $I_{OUT}$ = 0,1-3 A; 0,1 A/µs.*

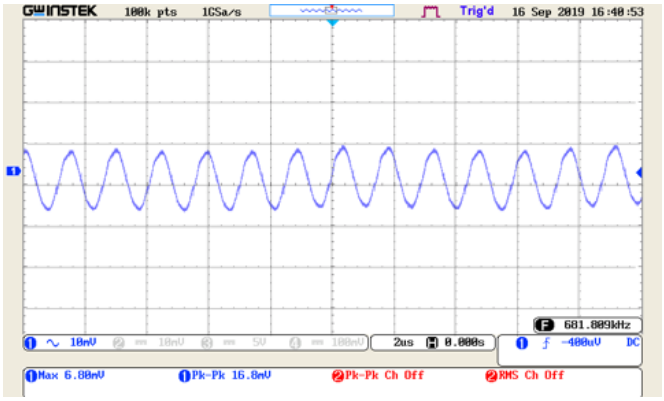
Top waveform - output voltage, 100 mV/div; bottom waveform - output current, 1 A/div; time - 100 µs/div.

$V_{IN}$ = 12V; $V_{OUT}$ = 5 V.

### 9.1.2. Output voltage ripple and noise




*Pic. 9. $I_{OUT}$ = 0,1 A.*

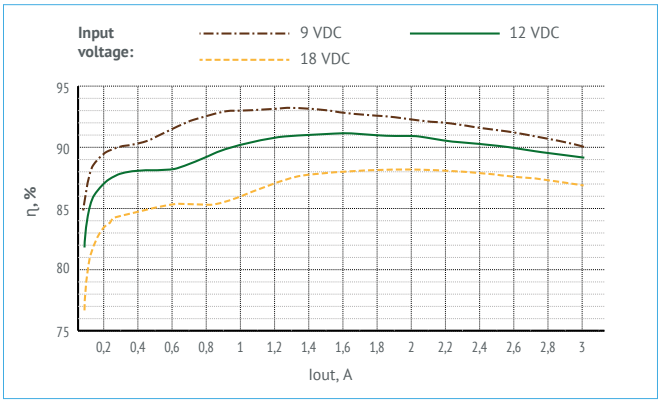



*Pic. 10. $I_{OUT}$ = 3 A.*

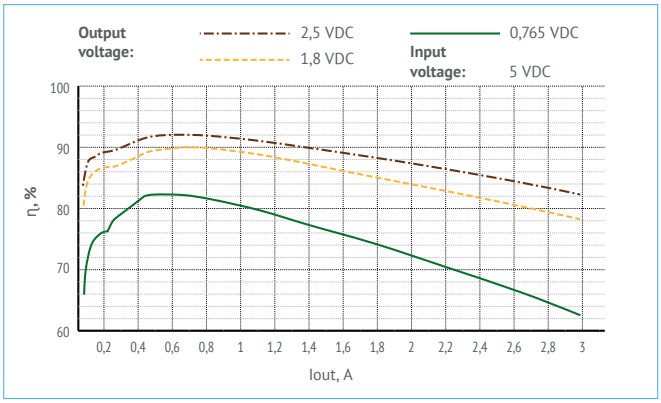
10 mV/div; time - 2 µs/div.

$V_{IN}$ = 12V; $V_{OUT}$ = 5 V.

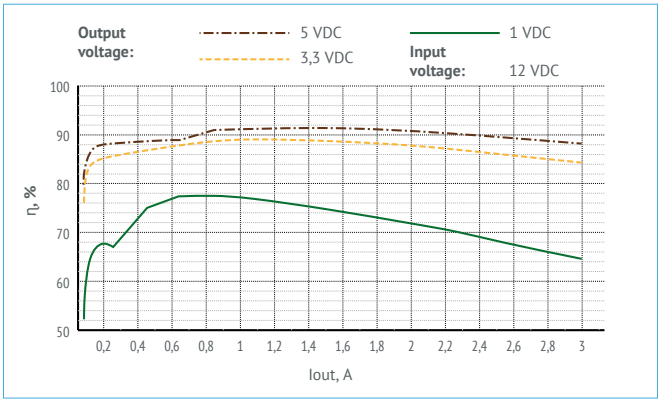
## 9.2. Efficiency




*Pic. 11. $V_{IN}$ = 9...18 V; $V_{OUT}$ = 5 V.*




*Pic. 13. $V_{IN}$ = 5 V; $V_{OUT}$ = 0,765 V; 1,8 V; 2,5 V.*




*Pic. 12. $V_{IN}$ = 12 V; $V_{OUT}$ = 1 V; 3,3 V; 5 V.*

# 10. Service functions

## 10.1. Output voltage setting

Output voltage setting in the range of 0,765 ... 7 V under the conditions $V_{OUT} \geqslant V_{IN} \times 0.07$ (V) and $V_{OUT} \leqslant V_{IN} \times 0,65$ (V) is done by selecting the resistance of the resistor connected between FB and AGND pins.

The resistance value of this resistor is calculated by the equation:

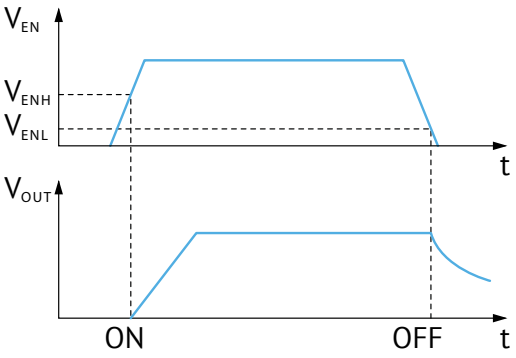
$$Rfb\ [kOhm] = \frac{7,65}{V_{OUT} - 0,765} - 1,1,$$

or it is selected from the table:

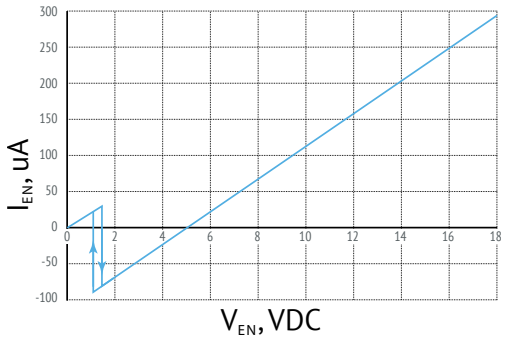
| $V_{OUT}$, V | 0,765 | 0,8 | 0,9 | 1 | 1,2 | 1,5 | 1,8 | 2,5 | 3,3 | 5,0 | 6,0 | 7,0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Rfb, kOhm | not connected | 215 | 54,9 | 30,9 | 16,2 | 9,2 | 6,19 | 3,28 | 1,91 | 0,698 | 0,357 | 0,124 |

## 10.2. On/off function

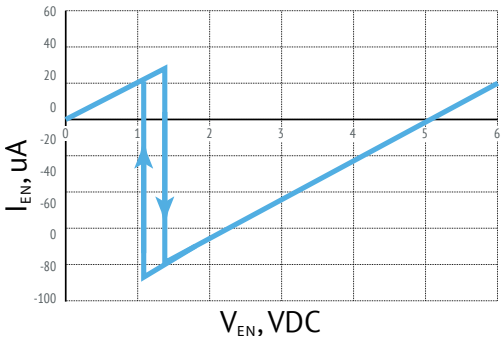
Converter is able to turn the output voltage on and off by a logic signal applied to EN pin referred to AGND pin. Low signal at EN pin (0,3 V or less) referred to AGND pin turns off the converter; high level signal (2,2 V ... $V_{IN}$) referred to AGND pin turns it on. In case of EN and $V_{IN}$ pins connection, converter will be turned on constantly. The signal level at EN pin should be changed in <2 ms.




*Pic. 14. ON/OFF depending on $V_{EN}$.*

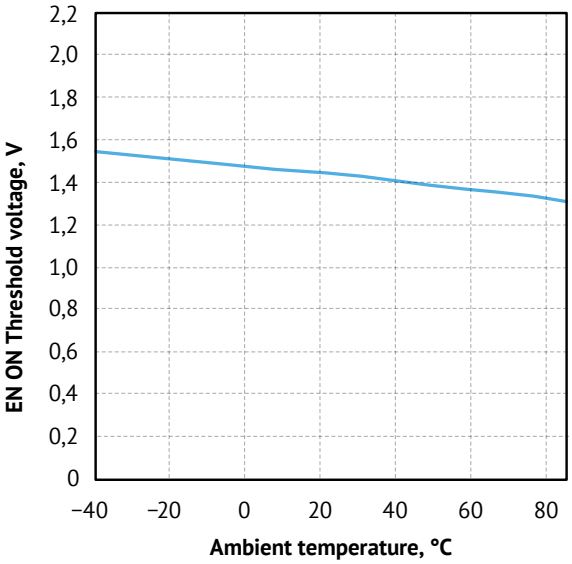



*Pic. 15. A typical curve of the sinking/soursing current on the EN pin, depending on the voltage on it. $V_{IN}$ = 18 VDC.*

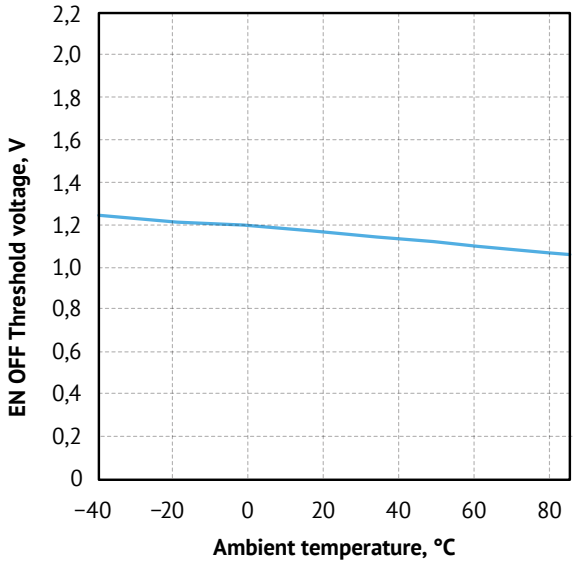



*Pic. 16. Typical hysteresis of switching on / off the module on the EN output.*

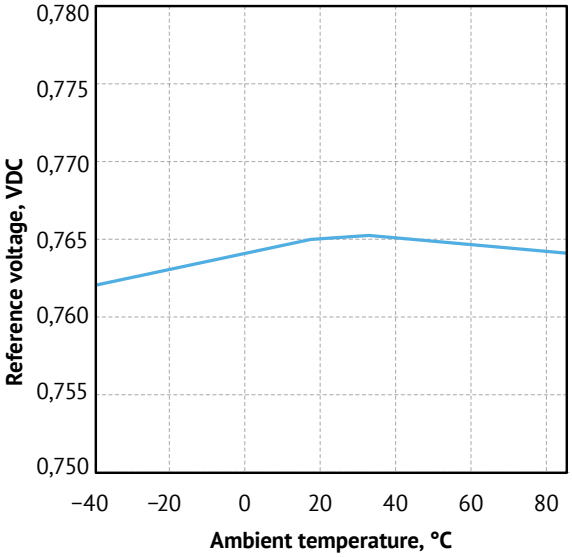
Turn-On *[Pic. 17]* and Turn-Off *[Pic. 18]* threshold vs. ambient temperature:




*Pic. 17. Temperature dependence of $V_{ENH}$ threshold.*



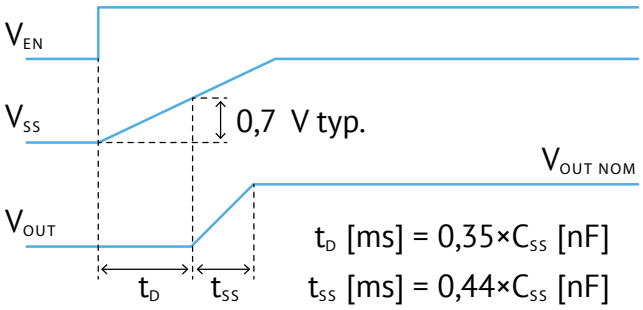

*Pic. 18. Temperature dependence of $V_{ENL}$ threshold.*




*Pic. 19. Typical dependence of the reference voltage on temperature. $V_{IN}$ = 12 VDC.*

## 10.3. «Soft start» function

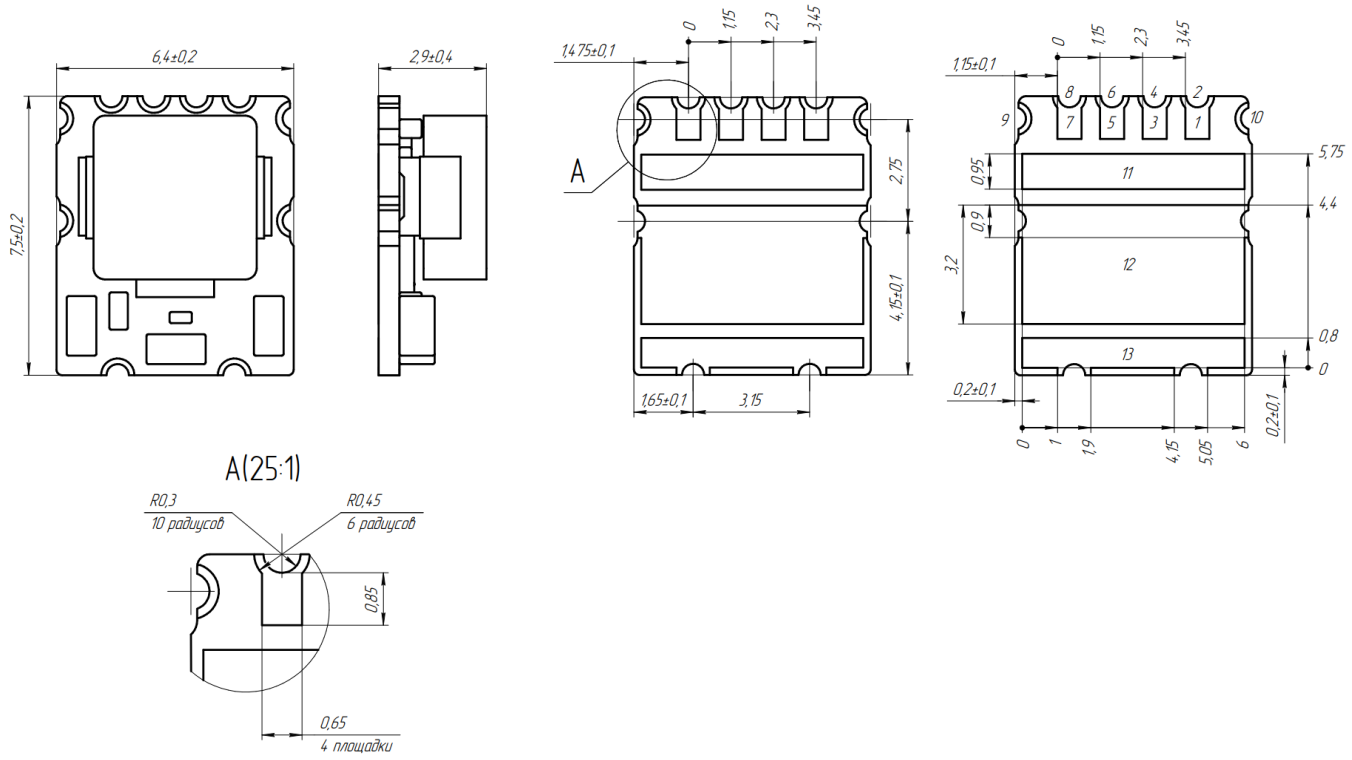
Using the «Soft start» function, you can prevent output overvoltage when converter is turned on; and reduce the starting current value. The output voltage rise time can be set by the $C_{SS}$ capacitor value, connected between SS and AGND pins. Converter's «soft-start» diagram, as well as the formulas for $C_{SS}$ capacitance selecting are presented in *[Pic. 20]* and in the table.




*Pic. 20. Converter's "soft-start" diagram.*

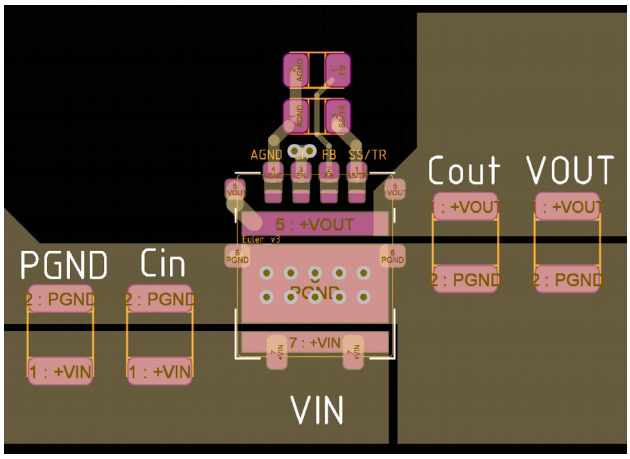
| $C_{SS}$, nF | 0,22 | 0,47 | 1 | 1,5 | 2,2 | 3,3 | 4,7 | 7,5 | 10 |
|---|---|---|---|---|---|---|---|---|---|
| $t_D$, ms | 0,08 | 0,16 | 0,35 | 0,53 | 0,77 | 1,16 | 1,65 | 2,63 | 3,5 |
| $t_{SS}$, ms | 0,1 | 0,21 | 0,44 | 0,66 | 0,97 | 1,45 | 2,07 | 3,3 | 4,4 |

# 11. Drawing

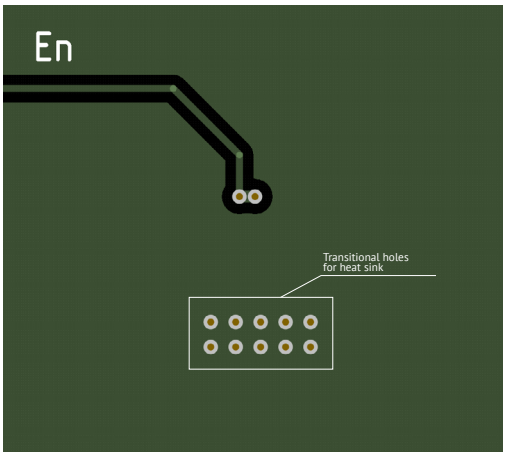



*Pic. 21. When mounting, it is recommended to use all contact pads, especially PGND, as it is used for heat conduction.*

## 11.1. Example of EULER layot

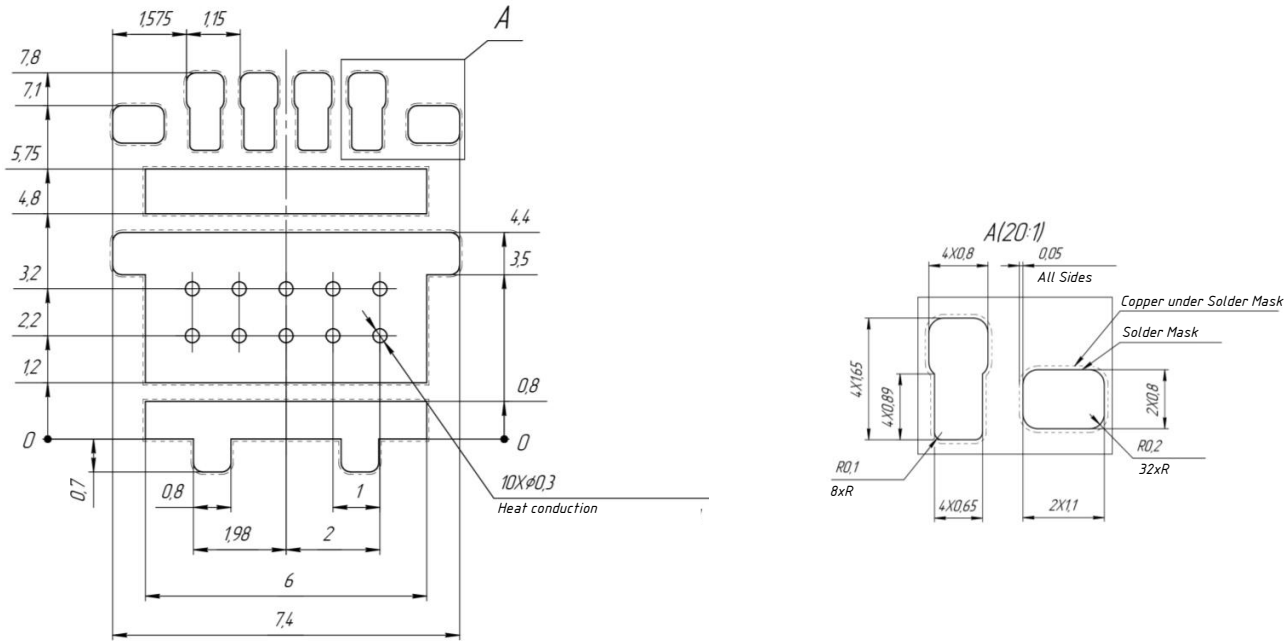



*Pic. 22. «Top» PCB (example).*



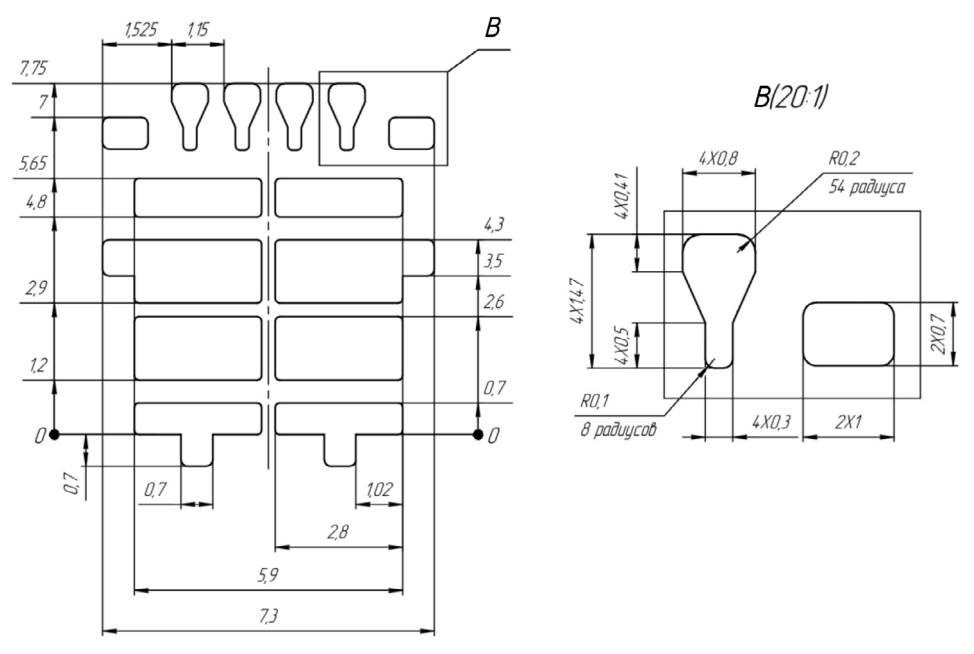

*Pic. 23. «Bottom» PCB (example).*

## 11.2. Dimensions of board layot




*Pic. 24. Land pattern example.*

## 11.3. Recommended stencil design



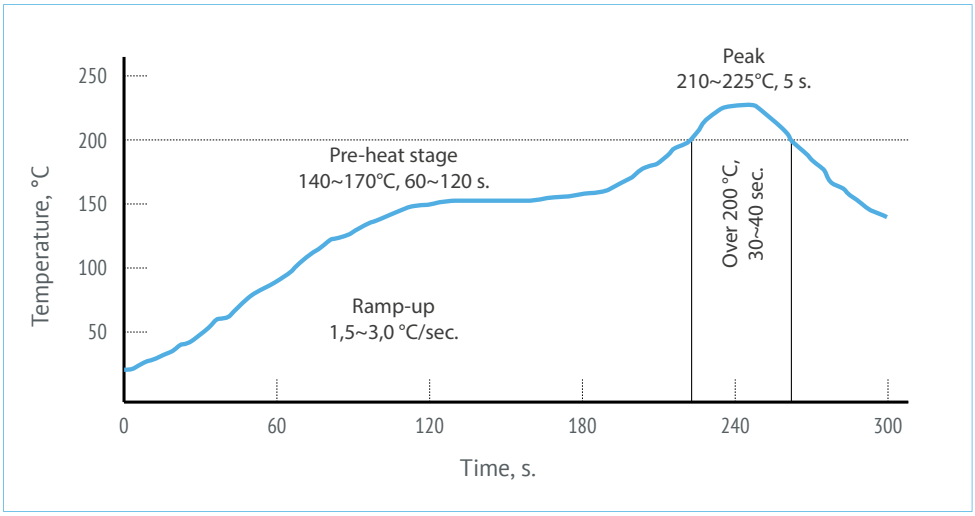

*Pic. 25. Solder paste example based on 0.1 mm thick stencil.*

# 12. Mounting on PCB

EULER mounting on PCB SHOULD be performed by surface mounting equipment. It is necessary to use soldering pastes with solder balls of at least Type 4 (20–38 microns) in alloys:

- Sn63, Pb37;
- Sn62, Pb36, Ag2;
- or Sn62.6, Pb36.8, Ag0.4, Sb0.2.

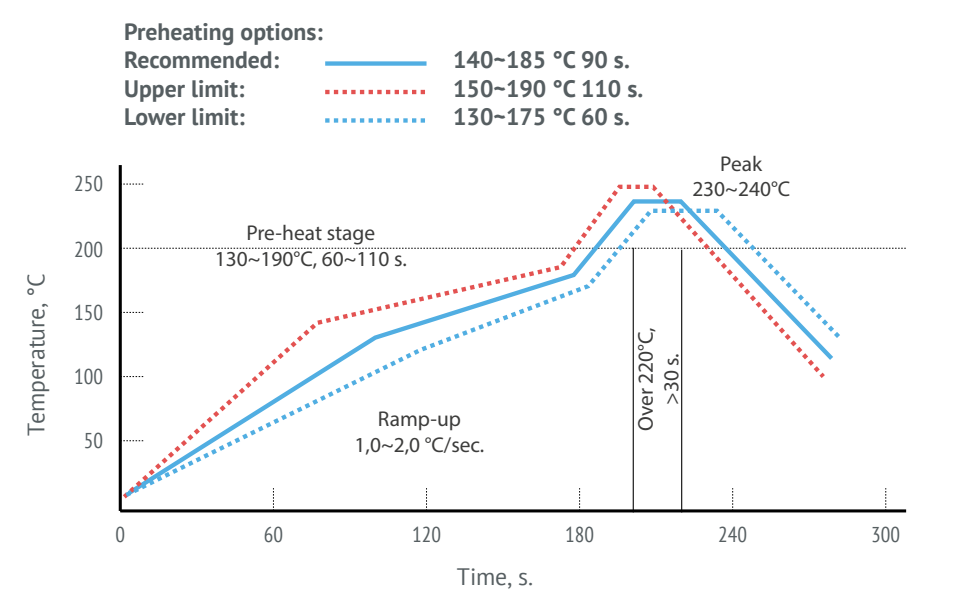
It is recommended to use KOKI SS58-M955LV paste.




*Pic. 26. Reflowing in a convection heating oven.*

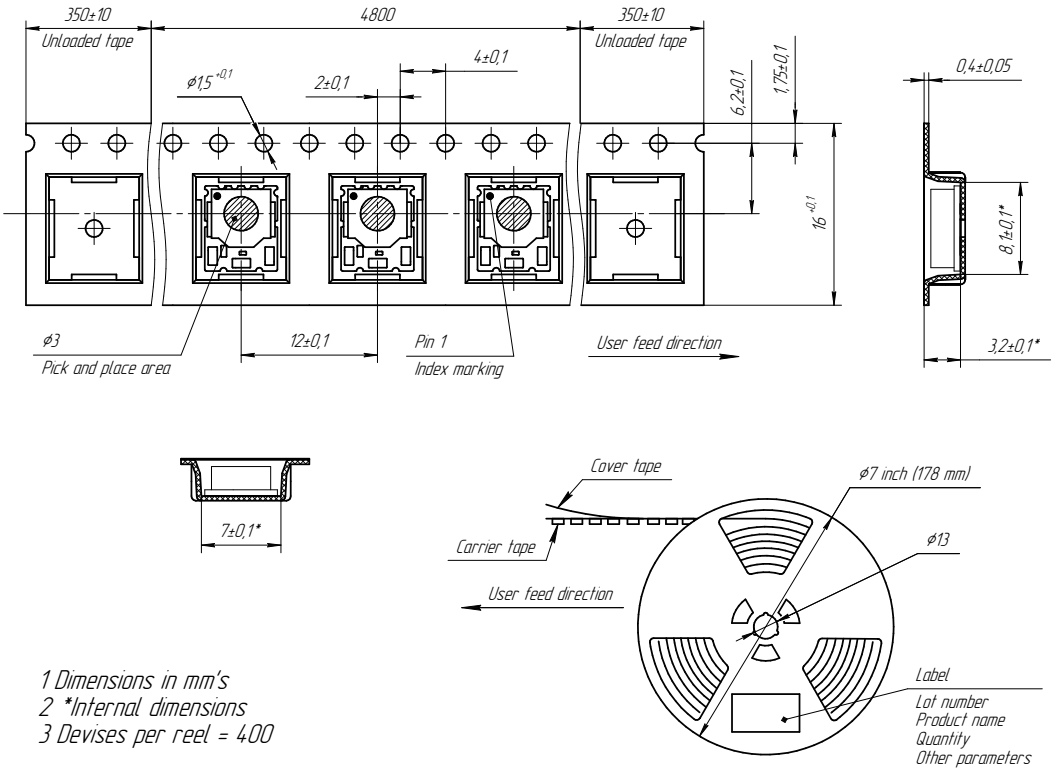
If it is necessary to use lead-free processes, installation should be carried out using solder pastes with solder balls of at least type 4 (20–38 microns) from alloys: Sn96.5; Ag3.0; Cu0.5 (SAC305)

It is recommended to use KOKI S3x58-G803 paste.




*Pic. 27. Reflowing in a convection heating oven.*

# 13. Packing information

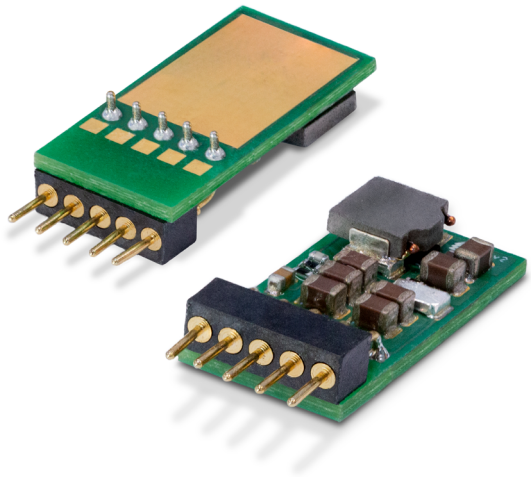



*Pic. 28. Packing information.*

# 14. Through hole design

It is possible to order design VNA3L0, 870, 0SP with pins for manual mounting on a printed circuit board (THD):

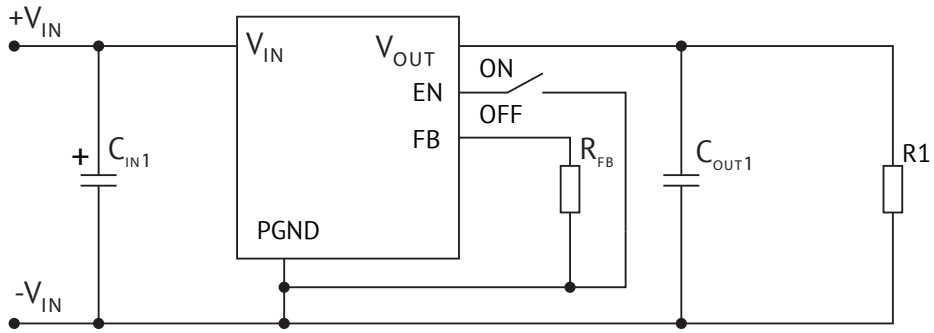
- version with partial circuit diagram *[]*;
- design includes EN and FB functions;
- the pin pitch is similar to the «TO220-5» package.



*Pic. 29. Appearance VNA3L0, 87, 0SP.*

*The location of the components in the photo may differ from the actual version.

# 15. Typical connection diagram



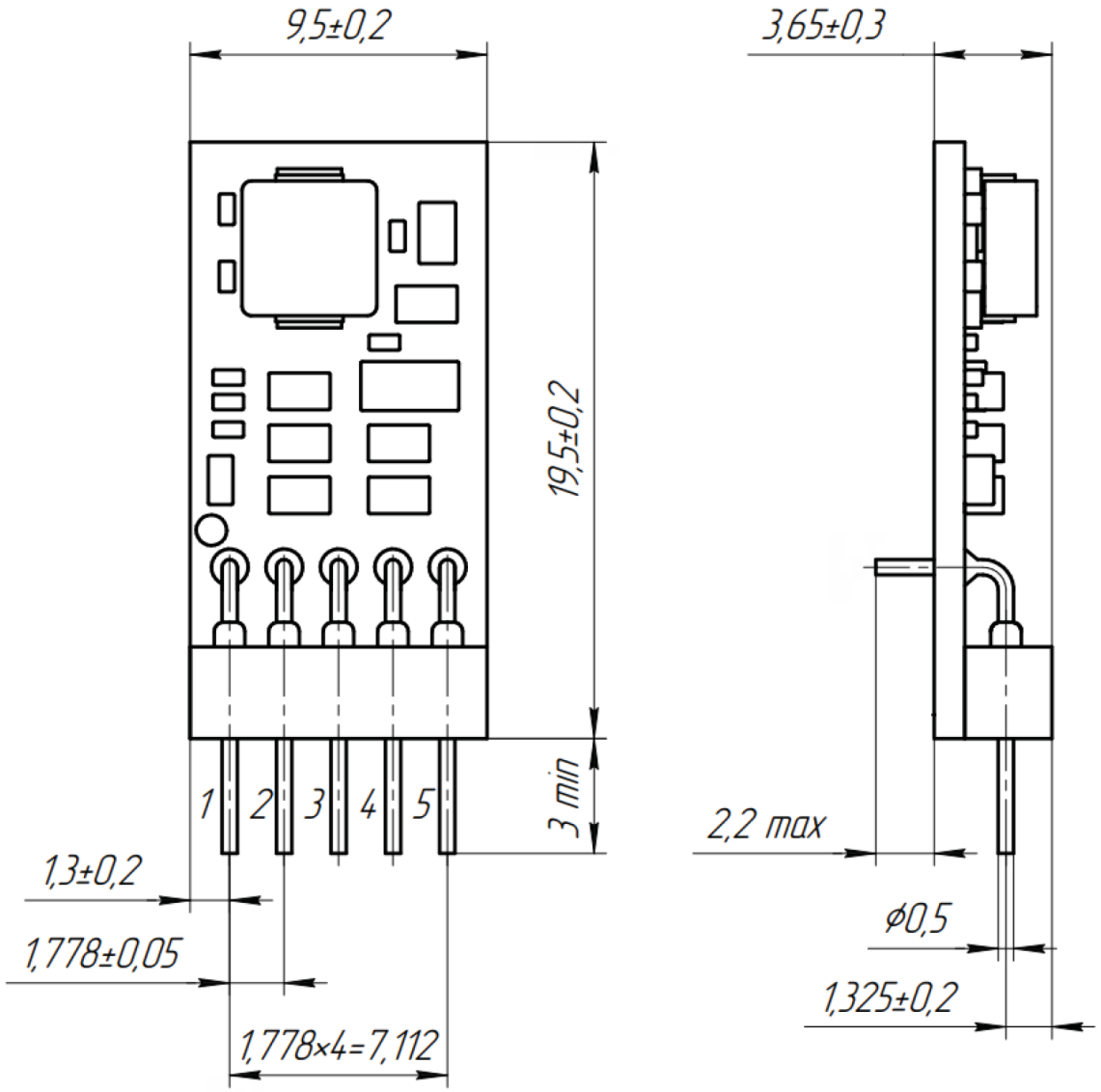

*Pic. 30. Typical connection diagram for VNA3L0, 87,0SP.*

**Table 2.** Description of connection diagram elements.

| | | |
|---|---|---|
| Cin1 | tantalum capasitor | 270 µF |
| Cout1 | tantalum capasitor | 10 µF |

$R_{FB}$ value is specified in *[10.1]*

# 16. Outline dimensions




*Pic. 31. Dimensional drawing and terminal designation VNA3L0,87,0SP.*

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**This datasheet is valid for the following units:** VNA3L0,87,0SQ, VNA3L0,87,0SP.